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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20040511

Application Number: 09/885,217
Filing Date: August 22, 2001
Appellant(s): KEETH ET AL.

Edward L. Pencoske
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/18/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 223, 225-237, 247-250, 496, 499 and 515 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5757175	Morishita et al.	05-1998
5838076	Zarrabian	11-1998
5448199	Park	05-1995
6127881	Tsay et al.	10-2000
5184031	Hayakawa	02-1993

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 223 and 511 are rejected under 35 U.S.C. 102(e) as being anticipated by Morishita et al (USP 5757175).

As to claim 223, figure 17 of Morishita et al. discloses a voltage reference circuit responsive to an external voltage (ExtVcc) for supplying a reference voltage (INVcc), the voltage reference circuit comprising an active reference circuit (VGR) for receiving the external voltage and for producing a reference signal (Vref) having a desired relationship with the external voltage.

Figure 19 shows the active reference circuit (VRG) comprising a current source (TP4) utilizing a current mirror for providing current to a diode stack (CVC) having an adjustable impedance, wherein the reference signal is dependent upon the external voltage. Column 2, lines 17-20, teaches that the reference voltage Vref is independent of the external power supply voltage EXVcc when the voltage EXVcc is at least at a prescribed voltage level. Thus, when the voltage EXVcc is lower than the prescribed voltage level, the reference voltage is dependent of the external supply voltage EXVcc.

Figure 17 further shows a unity gain amplifier (CMP, DT) responsive to the reference signal for producing the reference voltage.

As to clam 511, figures 17-19 show the reference signal is dependent upon the external voltage within a predetermined testing margined of error. Because Vref is generated from EXVcc, Vref is dependent on EXVcc within a certain voltage range (i.e. predetermined testing margined of error. Note that Vref is dependent on EXVcc when EXVcc is lower than the prescribed voltage level.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 225 and 496, 499, 500 and 514 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Zarrabian (USP 5838076).

As to claims 225 and 496, Morishita's figure 19 further shows the diode stack includes a plurality of transistors (Pra, PRb) connected in series, with each transistor's gate connected to a common potential (ground), and a plurality of fuses (La, Lb) each for shunting one of the transistors. Morishita et al. fails to show a plurality of switches each for selectively shunting one of the transistors. However, Zarrabian et al.'s figure 2 shows a apparatus that replacing fuses 23A-23c in figure 1 with switch circuits 54A-54E (combine with fuses 60A-60E and transistors 62A-62E) for the purpose of allowing different combinations of resistors be selectively shorted in both test and operating modes. Therefore, it would have been obvious to one having ordinary skill in the art to replace each of Morishita's fuses with Zarrabian's switches for the purpose of allowing different combinations of diodes be selectively shorted in both test mode and operating mode.

As to claim 499, the modified Morishita's reference further shows the switches are controlled by fuse (Zarrabian's 60A-60E).

As to claim 500, the modified Morishita's figure 19 shows the plurality of transistors includes a first plurality of field effect transistors and the plurality of switches includes a second plurality of field effect transistors (Zarrabian's 54A-54E).

As to claim 514, the modified Morishita et al.'s shows the reference signal is dependent upon the external voltage within a predetermined testing margin of error. Because Vref is generated from EXVcc, Vref is dependent on EXVcc within a certain voltage range (i.e. predetermined testing margined of error. Note that Vref is dependent on EXVcc when EXVcc is lower than the prescribed voltage level.

5. Claims 228-230 and 501-503 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. (USP 5757175) in view of Park (USP 5448199).

As to claims 228 and 501, Morishita et al's figures 17 and 19 show all limitation of the claims except for "a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value". However, Park's figure 3 shows a reference circuit having a pullup stage (100) for pulling up the reference voltage in a burn-in mode to check long term performance of the circuit under condition of high voltage and high temperature. Therefore, it would have been obvious to one having ordinary skill in the art to connect circuit Park's circuit 100, wherein circuit 100 is the "pull-up stage", to the output of the Morishita's unity gain amplifier for the purpose to check long term performance of the circuit under condition of high voltage and high temperature in burn-in mode.

As to claims 229 and 502, the modified Morishita et al. reference further shows the pull-up stage (Park's figure 3) includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 230 and 503, the modified Morishita et al. shows the reference voltage is the external voltage less a voltage drop across the plurality of diodes. Because of the diodes connected between the reference voltage terminal and the external terminal, the voltage drop across the diodes equal to VEXT – Vref. Thus, Vref = VEXT – Vdiodes.

6. Claims 231, 504, 512 and 515 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsay et al (USP 6127881) (newly cited) in view of Morishita et al. (USP 5757175).

As to claims 231 and 504, Tsay's figure 2 shows a multiplier circuit for for generating a voltage signal higher than a reference voltage (Vref). Thus, Tsay's figure 2 shows all limitations of the claims except for detail of the reference circuit.

However, Morishita's figure 17 shows a reference circuit comprising an active reference circuit (VRG) for receiving the external voltage and for producing a reference signal (Vref) having a desired relationship with the external voltage.

Morishita's figure 19 shows the active reference circuit comprising a current source (TP4) utilizing a current mirror for providing current to a diode stack (CVC) having an adjustable impedance, wherein the reference signal is dependent upon the external voltage. Column 2, lines 17-20, teaches that the reference voltage Vref is independent of the external power supply voltage EXVcc when the voltage EXVcc is at least at a prescribed voltage level. Thus, when the voltage EXVcc is lower than the prescribed voltage level, the reference voltage is dependent of the external supply voltage EXVcc;

Morishita's figure 17 further shows a unity gain circuit (CMP, DT).

Morishita's circuit has the advantage of generating a stable reference signal. Therefore, it would have been obvious to one having ordinary skill in the art use Morishita's figure 17 for Tsay's reference circuit for the purpose of having a stable reference signal.

As to claims 512 and 515, the combination of Tsay and Morishita references further shows the reference signal is dependent upon the external voltage within a predetermined testing margin of error. Because Vref is generated from EXVcc, Vref is dependent on EXVcc within a certain voltage range (i.e. predetermined testing margined of error. Note that Vref is dependent on EXVcc when EXVcc is lower than the prescribed voltage level.

7. Claims 232-233 and 505-506 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) (previous cited) in view Tsay et al (USP 6127881) and of Morishita et al. (USP 5757175).

As to claims 232 and 505, Hayakawa shows in figure 2 a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value and supplying a step down voltage when the external voltage is above the predetermined value. Thus, Hayakawa shows all limitations of the claim except for the detail of the internal stepdown circuit (13). However, the combination of Morishita et al's figure 17 and Tsay et al's figure 2 shows a detail of an internal step down circuit (see the rejection of claim 231). Morishita et al's figure 17 and Tsay et al's figure 2 having an advantage of providing a stable internal signal. Therefore, it would have been obvious to one having ordinary skill in the art to use the combination of Morishita et al's figure 17 and Tsay et al's figure 2 circuit for Hayakawa et al's internal stepdown circuit (13) for the purpose of providing a stable internal signal.

As to claims 233 and 506, Hayakawa et al.'s figure 2 shows the circuit for supplying includes a switch (14) for shorting a bus carrying the external voltage with a bus carrying the output voltage.

8. Claims 234-237, 247-250, 507-510 and 513 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayakawa (USP 5184031) (previous cited) in view of Tsay et al. (USP 6127881) and of Morishita et al. (USP 5757175) and Park (USP 5448199).

As to claim 234, the combination of Hayakawa, Tsay et al., and Morishita et al. references above shows all limitations of the claims except for "a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage

exceeds a second predetermined value". However, Park's figure 3 shows a reference circuit having a pullup stage (100) for pulling up the reference voltage in a burn-in mode to check long term performance of the circuit under condition of high voltage and high temperature. Therefore, it would have been obvious to one having ordinary skill in the art to connect circuit Park's circuit 100, wherein circuit 100 is the "pullup stage", to the output of the Morishita's unity gain amplifier for the purpose to check long term performance of the circuit under condition of high voltage and high temperature in burn-in mode.

As to claims 235 and 508, Park's figure 3 shows the pullup stage includes a plurality of diodes (61-63) connected between the external voltage and the reference voltage.

As to claims 236 and 509, the combination above shows the reference voltage is the external voltage less a voltage drop across the plurality of diodes. Because of the diodes connected between the reference voltage terminal and the external terminal. Therefore, the voltage drop across the diodes equal to VEXT – Vref. Thus, Vref = VEXT – Vdiodes.

As to claims 237 and 510, the combination of references above further shows the combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range. When the external voltage less than the threshold of the diode stack CVC of Morishita et al., the slop of Vref is the same as the slop of the external voltage.

Increases at a second slope substantially less than a slope of the external voltage during an operating range. When the external voltage greater than the threshold of the diode stack, diodes stack CVC clamp Vref at a level equal to the threshold of CVC.

Increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage (when external voltage greater than the break down voltage of the diode stack CVC).

Claim 247 recites similar limitations of claims 232-237. Therefore, it is rejected for the same reasons.

As to claim 248, Morishita et al.'s figure 19 shows the step generating a current (I) related to external voltage, apply a current to a circuit node (Vref), and draining the current from the circuit node through an adjustable impedance (CVC).

As to claim 249, the combination references above further shows the step of adjusting the impedance to modify the reference signal by open the switch La, Lb of Morishita et al.

As to claim 250, Morishita et al.'s figure 19 shows the step of adjusting the impedance includes the step of opening a fuse.

As to claim 513, the combination above further shows the reference signal is dependent upon the external voltage within a predetermined testing margin of error. Because Vref is generated from EXVcc, Vref is dependent on EXVcc within a certain voltage range (i.e. predetermined testing margined of error). Note that Vref is dependent on EXVcc when EXVcc is lower than the prescribed voltage level.

(11). Response to Argument

Appellants argue that "Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal". The Examiner respectfully disagrees. It is well known in the art that unity gain amplifier is an amplifier with a gain equal to one (1). The gain of amplifier circuit, which comprises elements

CMP and DT, is the ratio of INVCC voltage and Vref voltage (gain = Vout/Vin). As cited by Applicant, Morishita et al. states in column 2, lines 21-34, that "...This internal power supply down-converter therefore maintains the internal power supply voltage INVcc at the reference voltage Vref level". Thus, INVcc is equal to Vref. Therefore, the gain of the amplifier, which comprises elements CMP and DT, is one (1) or unity.

With respect to the arguments regarding in sections (1), (2), and (3) in pages 5-6, the Appellants argue that the modifications of Morishita et al. in view of Zarrabian, Tsay et al. in view of Morishita et al., and Hayakawa in view of Tsay, Morishita et al., and Park fail to teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal. However, as discussed above, Morishita et al.'s circuit, which comprises elements CMP and DT, is a unity gain amplifier. Therefore, the modifications of Morishita et al. in view of Zarrabian, Tsay et al. in view of Morishita et al., and Hayakawa in view of Tsay, Morishita et al., and Park show a unity gain amplifier that produces a reference voltage in response to a reference signal.

(12) Conclusion

Morishita discloses a circuit arrangement in figures 17 and 19 that meets all limitations of the appealed claims. As such, the rejections under 35 U.S.C. 102(e) and 103(a) are proper and should be sustained for the stated reasons above.

Respectfully submitted,

QT
May 21, 2004

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